REMARKS

This responds to the Office Action mailed on March 9, 2004.

Claims 3, 6, 12 and 13 are amended, claims 20, 21, and 22 are canceled, and no claims are added; as a result, claims 1-19 are now pending in this application. The amendments to the claims are fully supported by the specification as originally filed, and no new matter has been added. The amendments are made to clarify the claims and are not intended to limit the scope of equivalents to which any claim element may be entitled. Applicant respectfully requests reconsideration of the above-identified application in view of the amendments above and the remarks that follow.

Specification Objections

The title of the application was deemed not descriptive by the Examiner. The abstract of the disclosure was objected to due to informalities. The specification was objected to due to informalities.

The title, abstract and specification have been amended to correct the informalities.

Drawing Objections

The drawings were objected to due to informalities.

Replacement sheets for Figures 4, 5, and 6 are submitted herewith to correct the informalities.

Claim Objections

Claims 1, 7, 12, 17 and 20 were objected to because the Examiner was unclear on why "the plurality of arithmetic flags represent the status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items."

Claim 20 has been cancelled.

Applicant respectfully submits that the use of the term "status" is appropriate. As stated in the Applicant's specification, "FIG. 1A through 1D are representative examples of SIMD words utilized to indicate the arithmetic flags *associated* with data items being manipulated by a

processor having SIMD capability in the example embodiments of the present invention. . . ." The specification then describes different examples of that status that a flag may represent (for example, an overflow condition.)

Claims 3, 6, 12 and 13 were objected to due to informalities. Claims 3, 6, 12 and 13 are have been amended to correct the informalities.

Double Patenting Rejection

The Examiner pointed out that if claims 17-19 were to be allowed, claims 20-22 would then be objected to under 37 C.F.R. 1.75 as being a substantial duplicate thereof.

Claims 20-22 have been cancelled.

§112 Rejection of the Claims

Claims 12-16 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The preamble of claim 12 has been amended for clarity.

§102 Rejection of the Claims

Claims 1-4, 6-9, 12-14 and 17-22 were rejected under 35 USC § 102(e) as being anticipated by Wilson (U.S. 6,530,012).

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). Applicant respectfully submits that the claims are distinguishable over Wilson for the reasons argued below.

Claim 1. Applicant respectfully submits that the Office Action did not make out a *prima facie* case of anticipation against independent claim 1.

Applicant's claim 1 recites: "a combination function module that examines a plurality of arithmetic flags, determines field size of the plurality of arithmetic flags and based on the

determination of the field size, will combine the plurality of arithmetic flags into a single combined arithmetic flag variable. . ." (emphasis added).

Wilson does not teach each and every element of claim 1. Wilson relates to executing instructions on operands containing a plurality of packed objects in respective lanes of the operand (Wilson, Abstract). Figure 6 of Wilson describes a functional unit capable of executing ADD instructions (Wilson, column 7, lines 35- 55). Wilson shows the addition of two operands (SRC1 and SRC2) each with eight packed objects (b0 to b7) and Addition circuitry 44 with eight operators. Wilson describes how many condition codes are updated during particular type of SIMD operation (byte, half word, word) (Wilson, column 6, lines 43- 45, 46- 56, and 58- 65). However, Wilson does not describe a combination function module that "will combine the plurality of arithmetic flags into a *single combined* arithmetic flag variable."

Thus, Applicant respectfully submits that the Office Action fails to make out a *prima facie* case of anticipation against claim 1 for the above mentioned reasons, and reconsideration for allowance of claim 1 is respectfully requested. Claims 2- 4, and 6, which are dependent from claim 1, include all of the features of claim 1 and are therefore patentable over Wilson for at least the same reason.

Claim 7. Applicant respectfully submits that the Office Action did not make out a *prima facie* case of anticipation against independent claim 7.

Applicant's claim 7 recites "combining the plurality of arithmetic flags based on a function selected when a combination process is selected; and storing a result of the combining of the plurality of arithmetic flags in a destination register for access by the processor."

Wilson does not teach each and every element of claim 7. Wilson does not teach a "combination process." Fig. 6 of Wilson relates to a functional unit capable of executing ADD instruction on two source operands containing eight packed objects each (Wilson, column 7, lines 35- 40). Wilson describes how many condition codes are updated during particular type of SIMD operation (byte, half word, word) (Wilson, column 6, lines 43- 45, 46- 56, and 58- 65). Wilson relates to storage of the condition codes generated by considering the results of the addition operations carried out on packed objects in the source registers. The condition codes generated for the side of the machine where the instruction is being executed (Wilson, column 7,

lines 48- 65). Thus, Wilson does not teach each element of claim 7 for the reasons provided above. However, Wilson does not describe a combination process and "storing *a result of the combining of the plurality of arithmetic flags* in a destination register for access by the processor." (emphasis added).

Thus, Applicant respectfully submits that the Office Action fails to make out a *prima facie* case of anticipation against claim 7 for the above-mentioned reasons, and reconsideration for allowance of claim 7 is respectfully requested. Claims 8-9, which are dependent from claim 7, include all of the features of claim 7 and are therefore patentable over Wilson for at least the same reason.

Claim 12. Applicant respectfully submits that the Office Action did not make out a *prima facie* case of anticipation against independent claim 12.

Applicant's claim 12 recites: "combining the plurality of arithmetic flags based on a function selected when a combination process is selected. . ."

Wilson does not teach each and every element of claim 12 because Wilson does not teach combining the plurality of arithmetic flags. Wilson relates to storage of condition codes that are generated by considering the results of the addition operations carried out on packed objects in the source registers and that are generated for the side of the machine where the instruction is being executed (Wilson, column 7, lines 48- 65). Applicant's invention as claimed in claim 12 is directed extracting and combining a plurality of arithmetic flags that represent the status of a plurality of data items.

Thus, Applicant respectfully submits that the Office Action fails to make out a *prima facie* case of anticipation against claim 12 for the above mentioned reasons, and reconsideration for allowance of claim 12 is respectfully requested. Claims 13-14, which are dependent from claim 12, include all of the features of claim 12 and are therefore patentable over Wilson for at least the same reason.

Claim 17. Applicant respectfully submits that the Office Action did not make out a *prima facie* case of anticipation against independent claim 17.

Applicant's claim 17 recites: "determining a field size of the plurality of arithmetic flags on which to base a combination process. . ."

Wilson does not teach each and every element of claim 17. As described above, Wilson does not teach a "combination process." Fig. 6 of Wilson relates to a functional unit capable of executing ADD instruction on two source operands containing eight packed objects each (Wilson, column 7, lines 35- 40). Wilson describes how many condition codes are updated during particular type of SIMD operation (byte, half word, word) (Wilson, column 6, lines 43- 45, 46- 56, and 58- 65). Wilson relates to storage of the condition codes generated by considering the results of the addition operations carried out on packed objects in the source registers. However, Wilson does not describe a combination process.

Thus, Applicant respectfully submits that the Office Action fails to make out a *prima facie* case of anticipation against claim 17 for the above mentioned reasons, and reconsideration for allowance of claim 17 is respectfully requested. Claims 18- 9, which are dependent from claim 17, include all of the features of claim 17 and are therefore patentable over Wilson for at least the same reason.

Claim20. Claims 20, 21, and 22 are cancelled.

In addition, Applicant does not admit that Wilson is prior art, and reserves the right to swear behind it at a later date. Nevertheless, Applicant respectfully submits that the claims are distinguishable over Wilson for the reasons argued above.

§103 Rejection of the Claims

Claims 5, 10, 11, 15 and 16 were rejected under 35 USC § 103(a) as being unpatentable over Wilson in view of Bindloss et al. (U.S. 5,778,241).

Claim 5 which is dependent from claim 1 includes all of the features of claim 1, and is therefore patentable over Wilson and Bindloss for at least the same reasons as stated above for claim 1. Bindloss does not supply the feature of claim 1 which was missing from Wilson.

Claim 10- 11 which are dependent from claim 7 include all of the features of claim 7, and are therefore patentable over Wilson and Bindloss for at least the same reasons as stated above for claim 7. Bindloss does not supply the feature of claim 7 which was missing from Wilson.

Claim 15- 16 which are dependent from claim 12 include all of the features of claim 12, and are therefore patentable over Wilson and Bindloss for at least the same reasons as stated above for claim 12. Bindloss does not supply the feature of claim 12 which was missing from Wilson.

Conclusion

Applicant respectfully reconsideration and allowance of claim 1-19 in view of the above amendments and remarks. The Examiner is invited to telephone Applicant's attorney ((612) 349-9592) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

NIGEL C. PAVER

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

Date Sept. 9, 2004

By Ann M. McCrackin
Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9 day of September 2004.

Ann McCrackin

Name

Ann M. McCrackin

Signature